ANALOG DEVICES

Dual Precision JFET-Input Operational Amplifier

OP-215

FEATURES

- **High Slew Rate** ..... **10V/μs Min**
- **Fast Settling Time** ..... **0.9μs to 0.1% Typ**
- **Low Input Offset Voltage Drift** ..... **10μV/°C Max**
- **Wide Bandwidth** ..... **3.5MHz Min**
- **Temperature-Compensated Input Bias Currents**
- **Guaranteed Input Bias Current** ..... **18nA Max (125°C)**
- **Bias Current Specified Warmed-Up Over Temperature**
- **Low Input Noise Current** ..... **0.01pA/√Hz Typ**
- **High Common-Mode Rejection Ratio** ..... **86dB Min**
- **Pin Compatible With Standard Dual Pinouts**
- **125°C Temperature Tested DICE**
- **Models With MIL-STD-883 Class B Processing Available**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = 25°C V_{OS} MAX (mV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
1.0	OP215AJ*	OP215AZ*	–	–	MIL
1.0	OP215EJ	OP215EZ	OP215EP	–	COM
2.0	OP215BJ/883	OP215BZ/883	–	OP215BRC/883	MIL
2.0	OP215FJ	OP215FZ	OP215FP	–	COM
4.0	OP215CJ/883	OP215CZ/883	–	–	MIL
6.0	–	OP215GZ	OP215GP	–	XIND
6.0	–	–	OP215GS	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

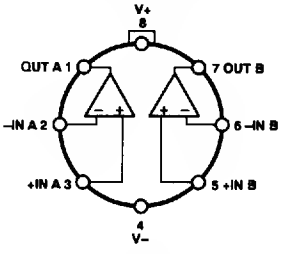
The OP-215 offers the proven JFET-input performance advantages of high speed and low input bias current with the tracking and convenience advantages of a dual op-amp configuration.

Low input offset voltages, low input currents, and low drift are featured in these high-speed amplifiers.

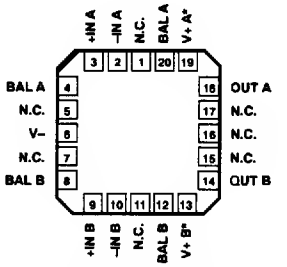
On-chip zener-zap trimming is used to achieve low V_{OS} while a bias-current compensation scheme gives a low input bias current at elevated temperatures. Thus the OP-215 features an input bias current of 18nA at 125°C ambient (not junction) temperature which greatly extends the application usefulness of this device.

Applications include high-speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocell

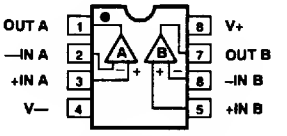
PIN CONNECTIONS



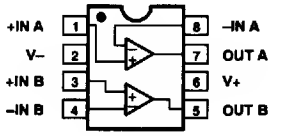
TO-99
(J-Suffix)



LCC 20-CONTACT
(RC-Suffix)
*V+ A & V+ B INTERNALLY CONNECTED

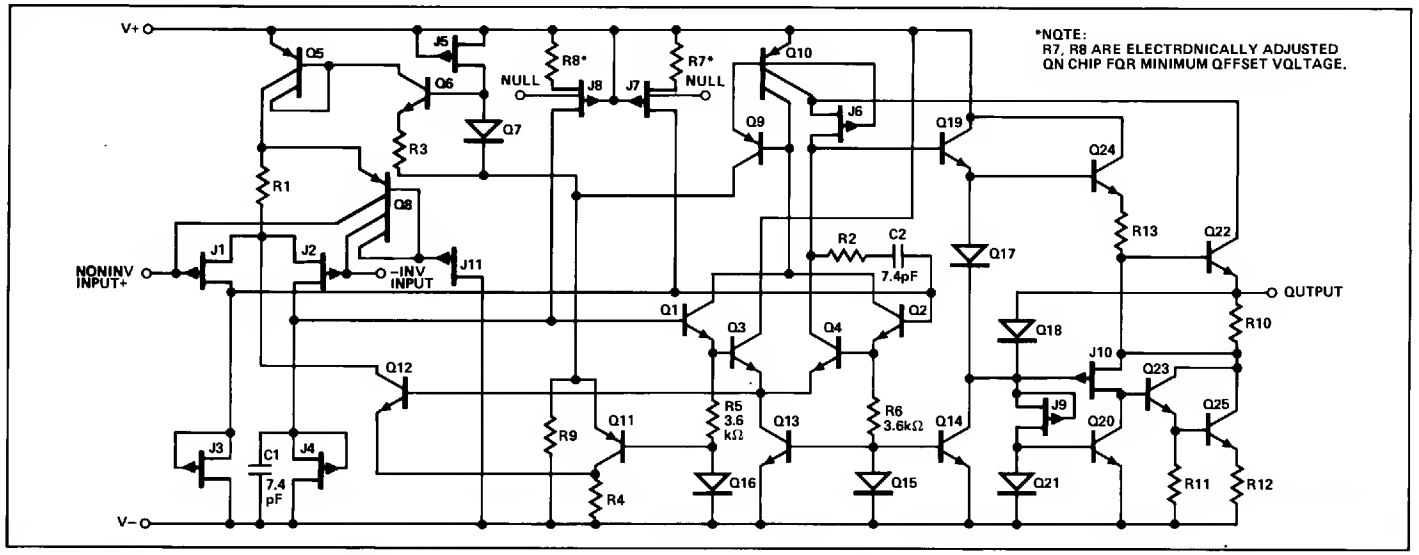


8-PIN CERDIP
(Z-Suffix)
8-PIN PLASTIC DIP
(P-Suffix)



8-PIN SO
(S-Suffix)

SIMPLIFIED SCHEMATIC (1/2 OP-215)



GENERAL DESCRIPTION *Continued*

amplifiers. For additional precision JFET op amps, see the OP-15/16/17 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- OP-215A, OP-215B, OP-215E, OP-215F (All DICE Except GR) ..... ±22V
- OP-215C, OP-215G (GR DICE Only) ..... ±18V

Operating Temperature Range
- OP-215A, OP-215B, OP-215C ..... −55°C to +125°C
- OP-215E, OP215F ..... 0°C to + 70°C
- OP-215G ..... −40°C to +85°C

Maximum Junction Temperature (T_j) ..... +150°C

Differential Input Voltage
- OP-215A, OP-215B, (All DICE Except GR) ..... ±40V
- OP-215E, OP-215F, (All DICE Except GR) ..... ±40V
- OP-215C, OP-215G, (GR DICE Only) ..... ±30V

Input Voltage
- OP-215A, OP-215B, (All DICE Except GR) ..... ±20V
- OP-215E, OP-215F, (All DICE Except GR) ..... ±20V
- OP-215C, OP-215G, (GR DICE Only) ..... ±16V

(Unless otherwise specified, the absolute maximum negative input voltage is equal to one volt more positive than the negative power supply voltage.)

Output Short-Circuit Duration ..... Indefinite

Storage Temperature Range ..... −65°C to +150°C

Lead Temperature (Soldering, 60 sec) ..... 300°C

Junction Temperature (T_j) ..... −65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	145	16	°C/W
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	150	41	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-215A/E			OP-215B/F			OP-215C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.2	1.0	—	0.8	2.0	—	2.0	4.0	mV
		'G' Grade	—	—	—	—	—	—	—	2.5	6.0	
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)	—	3	50	—	3	50	—	3	100	pA
		Device Operating	—	5	100	—	5	100	—	5	200	
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)	—	±15	±100	—	±15	±200	—	±15	±300	pA
		Device Operating	—	±18	±300	—	±18	±400	—	±18	±600	
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	500	—	75	220	—	50	200	—	V/mV
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
		$R_L = 2k\Omega$	±11	±12.7	—	±11	±12.7	—	±11	±12.7	—	
Supply Current	I_{SY}		—	6.0	8.5	—	8.0	8.5	—	7.0	10.0	mA
		'G' Grade	—	—	—	—	—	—	—	7.0	12.0	
Slew Rate	SR	$A_{VCL} = +1$	10	18	—	7.5	18	—	5	15	—	V/μs
Gain Bandwidth Product	GBW	(Note 3)	3.5	5.7	—	3.5	5.7	—	3.0	5.4	—	MHz
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	—	13	—	—	13	—	—	12	—	MHz
Settling Time	t_S	to 0.01%	—	2.3	—	—	2.3	—	—	2.4	—	μs
		to 0.05% (Note 2)	—	1.1	—	—	1.1	—	—	1.2	—	
		to 0.10%	—	0.9	—	—	0.9	—	—	1.0	—	
Input Voltage Range	IVR		+10.2	+14.8	—	+10.2	+14.8	—	+10.1	+14.8	—	V
			−10.2	−11.5	—	−10.2	−11.5	—	−10.1	−11.5	—	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm$IVR A, B, C Grades	86	100	—	86	100	—	82	96	—	dB
		E, F, G Grades	82	100	—	82	100	—	80	96	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$	—	10	51	—	10	80	—	—	—	μV/V
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	18	100	
Input Noise Voltage Density	e_n	$f_O = 100Hz$	—	20	—	—	20	—	—	20	—	$nV/\sqrt{Hz}$
		$f_O = 1000Hz$	—	15	—	—	15	—	—	15	—	
Input Noise Current Density	I_n	$f_O = 100Hz$	—	0.01	—	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
		$f_O = 1000Hz$	—	0.01	—	—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}		—	3	—	—	3	—	—	3	—	pF

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215A MIN	OP-215A TYP	OP-215A MAX	OP-215B MIN	OP-215B TYP	OP-215B MAX	OP-215C MIN	OP-215C TYP	OP-215C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.5	2.0	—	1.5	3.0	—	3.0	8.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	—	3	10	—	3	10	—	6	—	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	3	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_j = +125°C$	—	0.8	8	—	0.8	8	—	1.0	12	nA
		$T_A = +125°C$, Device Operating	—	1.2	14	—	1.2	14	—	1.5	22	
Input Bias Current (Note 1)	I_B	$T_j = +125°C$	—	±1.5	±10	—	±1.5	±10	—	±1.8	±15	nA
		$T_A = +125°C$, Device Operating	—	±2.2	±18	—	±2.2	±18	—	±2.7	±28	
Input Voltage Range	IVR		+10.2	+14.6	—	+10.2	+14.6	—	+10.1	+14.6	—	V
			−10.2	−11.3	—	−10.2	−11.3	—	−10.1	−11.3	—	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	82	97	—	82	97	—	80	93	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$	—	10	100	—	15	100	—	—	—	µV/V
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	23	126	
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	30	110	—	30	110	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$ for E/F Grades, $-40°C \le T_A \le +85°C$ for G Grade, unless otherwise noted.

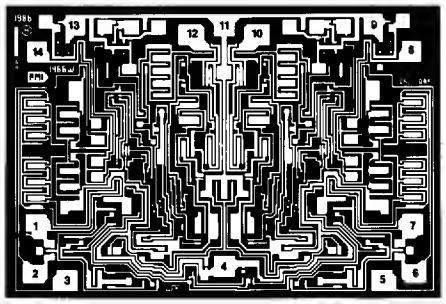
PARAMETER	SYMBOL	CONDITIONS	OP-215E MIN	OP-215E TYP	OP-215E MAX	OP-215F MIN	OP-215F TYP	OP-215F MAX	OP-215G MIN	OP-215G TYP	OP-215G MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.4	1.65	—	1.4	2.65	—	3.5	8.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	—	3	15	—	3	15	—	6	—	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	3	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_j = +70°C$	—	0.06	0.45	—	0.06	0.45	—	0.08	0.65	nA
		$T_A = +70°C$, Device Operating	—	0.08	0.80	—	0.08	0.80	—	0.10	1.2	
Input Bias Current (Note 1)	I_B	$T_j = +70°C$	—	±0.12	±0.70	—	±0.12	±0.70	—	±0.14	±0.9	nA
		$T_A = +70°C$, Device Operating	—	±0.16	±1.40	—	±0.16	±1.40	—	±0.19	±1.8	
Input Voltage Range	IVR		+10.2	+14.7	—	+10.2	+14.7	—	+10.1	+14.7	—	V
			−10.2	−11.4	—	−10.2	−11.4	—	−10.1	−11.3	—	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	80	98	—	80	98	—	76	94	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$	—	13	100	—	13	100	—	—	—	µV/V
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	20	159	
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	50	180	—	50	180	—	35	130	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs. T_j and I_B vs. T_A. PMI has a bias current compensation circuit which gives improved bias current and bias current over temperature vs. standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Sample tested.

OP-215

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. NULL (A)
4. V–
5. NULL (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. NULL (B)
9. V+
10. V_O (B)
11. V+
12. V_O (A)
13. V+
14. NULL (A)

ALL V+ PADS ARE INTERNALLY CONNECTED.

DIE SIZE 0.110 × 0.075 inch, 8250 sq. mils
(2.79 × 1.91 mm, 5.33 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-215N, OP-215G and OP-215GR devices; $T_A = 125°C$ for OP-215NT and OP-215GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215NT LIMIT	OP-215N LIMIT	OP-215GT LIMIT	OP-215G LIMIT	OP-215GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	2	1	3	2	6	mV MAX
Input Bias Current	I_B		±18	—	±18	—	—	nA MAX
Input Offset Current	I_{OS}		14	—	14	—	—	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 2k\Omega$	30	150	30	75	50	V/mV MIN
Input Voltage Range	IVR		±10.2	±10.2	±10.2	±10.2	±10.1	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	82	86	82	86	82	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10$ to $\pm 16V$ $V_S = \pm 10$ to $\pm 15V$	100 —	51 —	100 —	80 —	— 100	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 —	±12 ±11	±12 —	±12 ±11	±12 ±11	V MIN
Supply Current	I_{SY}		—	8.5	—	8.5	12.0	mA MAX

NOTES:
For 25°C characteristics of NT & GT devices, see N & G characteristics respectively.

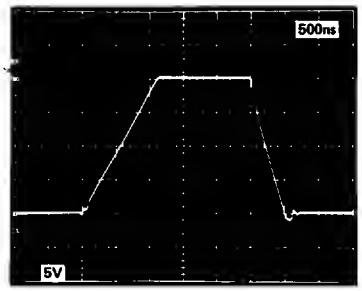
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

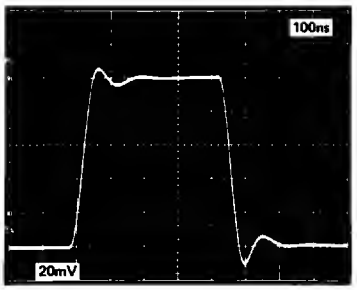
PARAMETER	SYMBOL	CONDITIONS	OP-215NT TYPICAL	OP-215N TYPICAL	OP-215GT TYPICAL	OP-215G TYPICAL	OP-215GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled $R_p = 100k\Omega$	2	2	3	3	4	μV/°C
Average Input Offset Voltage Drift	TCV_{OSn}	Nulled $R_P = 100k\Omega$	0.5	0.5	1	1	2	μV/°C
Input Offset Current	I_{OS}		3	3	3	3	3	pA
Input Bias Current	I_B		±15	±15	±15	±15	±15	pA
Slew Rate	SR	$A_{VCL} = +1$	17	17	16	16	15	V/μs
Settling Time	t_S	to 0.01% to 0.05% to 0.10%	2.2 1.1 0.9	2.2 1.1 0.9	2.3 1.1 0.9	2.3 1.1 0.9	2.4 1.2 1.0	μs
Gain Bandwidth Product	GBW		6.0	6.0	5.7	5.7	5.4	MHz
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	14	14	13	13	12	MHz
Input Noise Voltage Density	e_n	$f_O = 100Hz$ $f_O = 1000Hz$	20 15	20 15	20 15	20 15	20 15	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 100Hz$ $f_O = 1000Hz$	0.01	0.01	0.01	0.01	0.01	$pA/\sqrt{Hz}$
Input Capacitance	C_{IN}		3	3	3	3	3	pF

TYPICAL PERFORMANCE CHARACTERISTICS

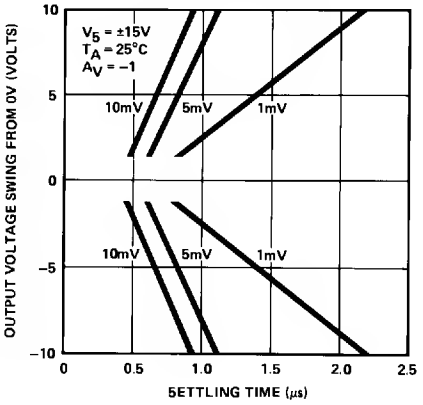
LARGE-SIGNAL TRANSIENT RESPONSE



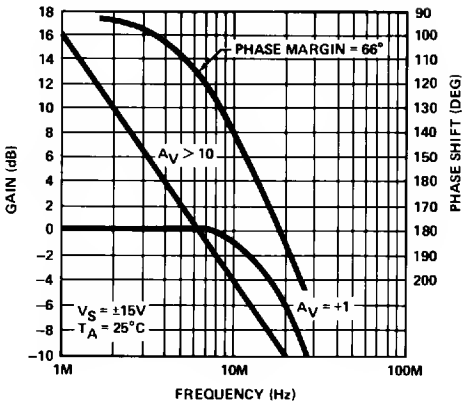
SMALL-SIGNAL TRANSIENT RESPONSE



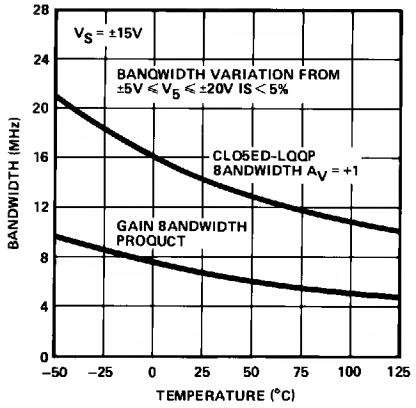
SETTLING TIME



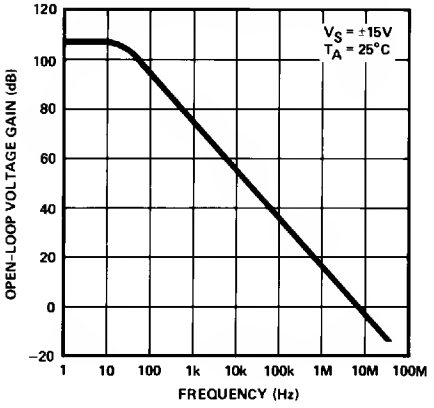
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



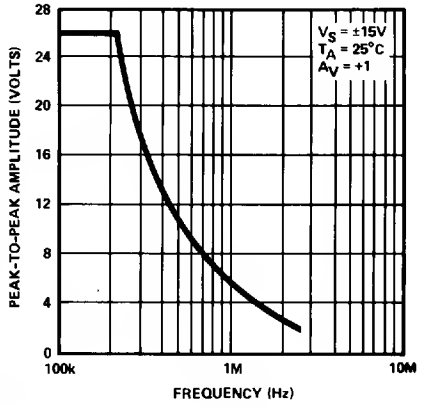
BANDWIDTH vs TEMPERATURE



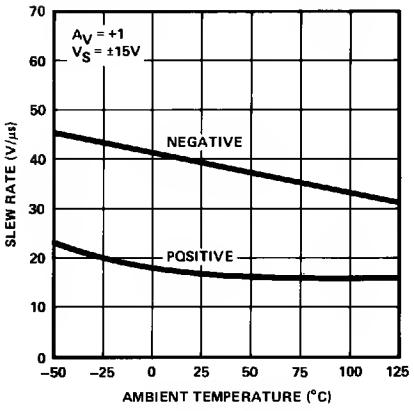
OPEN-LOOP FREQUENCY RESPONSE



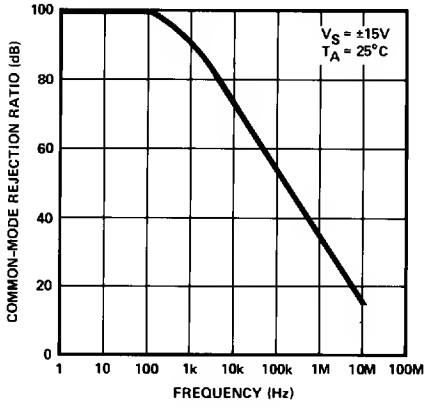
MAXIMUM OUTPUT SWING vs FREQUENCY



SLEW RATE vs TEMPERATURE



COMMON-MODE REJECTION RATIO vs FREQUENCY



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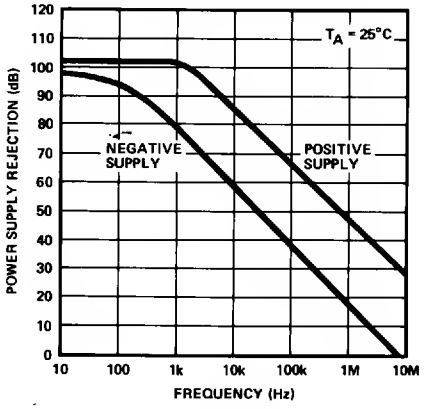
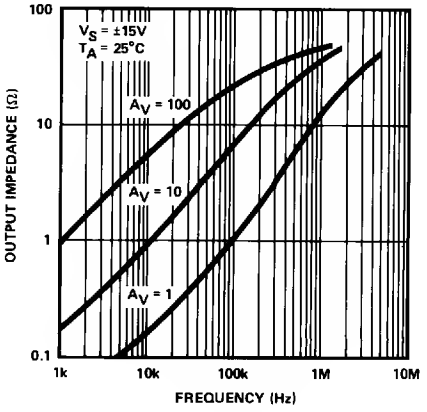
TYPICAL PERFORMANCE CHARACTERISTICS

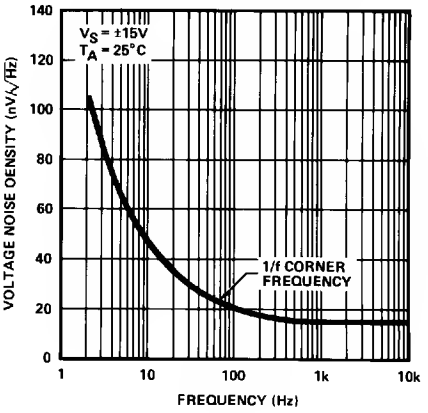
POWER SUPPLY REJECTION vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

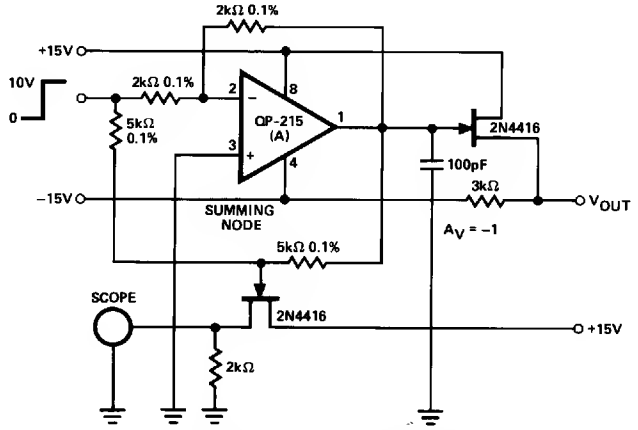


VOLTAGE NOISE DENSITY vs FREQUENCY



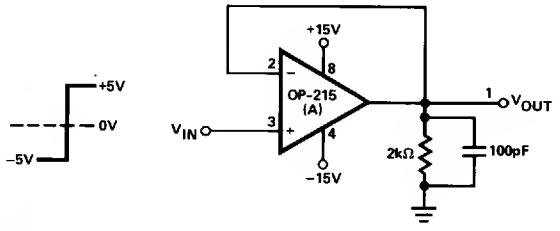
BASIC CONNECTIONS

SETTLING TIME TEST CIRCUIT



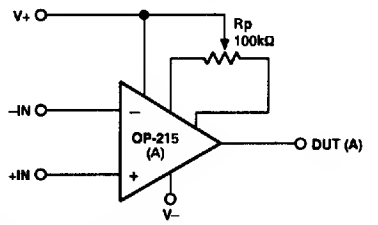
(PINOUT FOR "J," "Z" AND "P" PACKAGES ONLY)

SLEW RATE TEST CIRCUIT



(PINOUT FOR "J," "Z" AND "P" PACKAGES ONLY)

INPUT OFFSET VOLTAGE NULLING

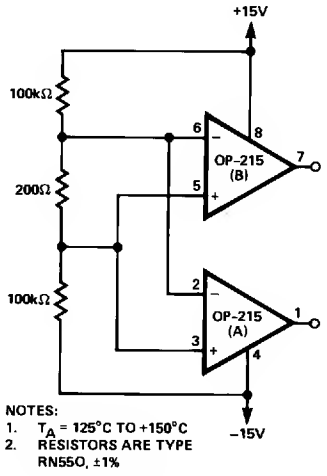


NOTE:
V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10kΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100kΩ POTENTIOMETER.

(DICE ONLY)

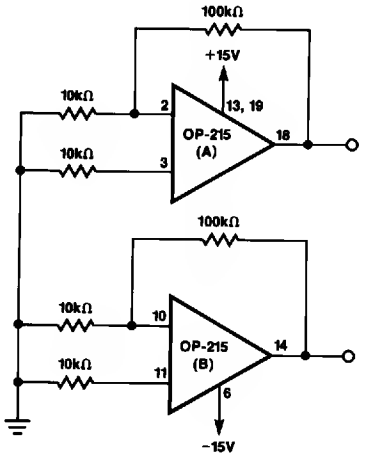
BASIC CONNECTIONS

BURN-IN CIRCUIT



NOTES:
1. T_A = 125°C TO +150°C
2. RESISTORS ARE TYPE RN55O, ±1%

("J," "Z" AND "P" PACKAGES ONLY)



("RC" PACKAGE)

APPLICATIONS INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback-pole time constant.